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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,787	12/02/2003	Michael J. Koster	SUN-P8985-SPL	6112

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EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 06/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,787	KOSTER ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-12 and 14-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-12 and 14-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the After-Final Amendment, filed 6/8/2006. Claims 1-3,5-12, and 13-20, are presented for examination and are currently pending.

In the response to this Office action, the Examiner politely requests that support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line numbers in the specification and/or drawing figure(s). This will assist the Examiner in prosecuting this application.

Response to Amendment/Arguments

Applicant's amendment to the claims (incorporating the subject matter of claims 4/13 into independent claims 1,10, 19, and 20) and arguments regarding the allowability over the prior art of record (pages 7-8 of the response) have been fully considered and are persuasive. Therefore, the corresponding claim rejections have been withdrawn. However, upon further consideration, new grounds of rejection is made in view of Ang (U.S. Patent Application Publication No. 2003/0079085) as discussed in detail below.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the --initializing mechanism--, --monitoring mechanism--, --protocol switching mechanism-- (all of claims 10 and 19), and the --locking mechanism-- (claim 16) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

The drawings are further objected to because figure 1 is currently labeled as --Prior Art--; however, as disclosed in Applicant 's specification (¶21), the figure is stated to be an embodiment of Applicant's invention. Clarification and/or correction is required.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 20 is objected to because of the following informalities:

As per claim 20, the claim's limitations recite the elements or terms of an --initialization means--, --monitoring means--, and a --protocol switching means--, none of which are contained in Applicant's specification as originally filed. Applicant is reminded of 37 C.F.R. 1.75 (d)(1) which states that the claim or claims must conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description. (See 1.58(a).)

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 7 and 16 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 7 and 16 both claim, when deciding whether or not to "lock" a cache into the write-invalidate protocol, a determination regarding the "modules" of a shared memory multiprocessor. Applicant's specification as originally filed contains zero description regarding such a "module," save for mentioning the "module" element in the Summary of the Invention

(¶18 of Applicant's specification). For example, it is not readily apparent to one having ordinary skill in the art if this "module" contained in the shared memory multiprocessor is a cache itself, a portion of a cache (i.e. specific banks, sets, ways, etc of a cache), a cache controller, a processor itself, or another part (either software or hardware) of an individual processor or of the multi-processor system that for some reason restricts the respective "module" from participating in a write-broadcast policy with the other processors of the multiprocessor shared memory system. Nonetheless, for the purposes of examination, the Examiner has considered the "module" to be a portion of a cache.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7,8,17, and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding the aforementioned claims, it is not apparent to the Examiner how a protocol can "send a message" to either update or invalidate, as a protocol is simply a collection of state machines (software code) that is implemented on a processor (in this case a multiple processors of the multi-processor system). It is the Applicant's responsibility to particularly point out and distinctly claim the subject matter that is regarded as his invention. Nonetheless, for the purposes of examination, the Examiner has considered the hardware system [associated with the local cache] (i.e. the processor or the cache controller, etc.) that is responsible for implementing the invalidation/broadcasting protocols to be the element that

"sends a message" (invalidation or broadcast) to other caches in a shared memory multiprocessor when a given cache line is updated in a local cache.

The following is a quotation of the fourth paragraph of 35 U.S.C. 112:

> Subject to the following paragraph, a claim in dependent form shall contain a reference to a claim previously set forth and then specify a further limitation of the subject matter claimed.

Claims 2 and 11 are rejected under 35 U.S.C. 112, fourth paragraph, as failing to further limit the claimed subject matter. Claims 2 and 11 both claim **monitoring the dynamic behavior of the cache on a cache-line by cache-line basis**. Such a limitation is currently present in base claims 1 and 10, respectively, in that "monitoring dynamic behavior of the cache maintains a count ... for each cache line." Therefore, the "monitoring of the dynamic behavior of the cache on a cache-line by cache-line basis" is already present in the claim scope.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3,5,6,8-12,14,15, and 17-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Ang (U.S. Patent Application Publication No. 2003/0079085).

As per claims 1,10, and 20, Ang teaches **initializing a cache to operate using a write-invalidate protocol** (¶20), **monitoring a dynamic behavior of the cache during program execution** (¶65), **wherein monitoring the dynamic behavior of the cache involves maintaining a count for each cache line of the number of cache line invalidations the cache line has been subject to during program execution and if the dynamic behavior indicated that better performance can be achieved using a wrote-broadcast protocol, switching the cache to operate using the write-broadcast protocol** (¶48). In ¶48, Ang teaches when deciding to transition from the invalidation to the update protocol, which is known in the art to be synonymous with the write-broadcast protocol (¶3), the memory-side coherence engine tracks the frequency (i.e. the number of occurrences, thereby which a counter is inherent) of cache-line invalidations. When the frequency of the invalidations reaches a threshold, the cache coherence protocol is dynamically switched from a write-invalidation scheme to a write-update (or write-broadcast) scheme.

As per claims 2 and 11, Ang teaches **monitoring the dynamic behavior of the cache on a cache-line by cache-line basis** (¶48), as the frequency of invalidations are maintained for each of the individual cache-lines.

As per claims 3 and 12, Ang teaches **switching to the write-broadcast** (i.e. the write-update) **protocol on a cache-line by cache-line basis** (¶48).

As per claims 5 and 14, Ang teaches **if the number of cache line invalidations indicates that a given cache line is updated frequently, switching the cache line to operate under the write-broadcast protocol** (write-update) in ¶48. Specifically, Ang teaches if the frequency of invalidations for a particular cache-line is frequent (i.e. above an inherent threshold), then the coherency policy for that particular cache line is changed to a write-update policy.

As per claims 6 and 15, Ang teaches **wherein if a given cache line is using the write-broadcast protocol and the number of cache line updates indicates that the given cache line is not being contended for by multiple processors** (i.e. only one processor is updating the cache line, as specifically claimed in claim 15)**, switching the given cache line back the write-invalidation protocol** (¶48).

As per claims 8 and 17, Ang teaches **the** [processor implementing a] **write-invalidate protocol sends an invalidation message to other caches in a shared memory multiprocessor when a given cache line is updated in a local cache** (¶20). Further the Applicant's Admitted Prior Art (herein "APA") teaches that such a limitation is inherent in write-invalidation protocols (¶6 of Applicant's specification).

As per claims 9 and 18, Ang teaches **the** [processor implementing a] **write-broadcast protocol broadcasts an update to other caches in a shared memory multiprocessor when**

the given cache line is updated in a local cache (¶3). Further, the APA teaches that such a limitation is inherent in write-broadcast (i.e. write-updating) protocols (¶9).

As per claim 19, the rejection follows the rejection for claims 1, 10, and 20 set forth above. Further, Ang teaches **a plurality of processors** (abstract, and labeled 102 in figure 1), **wherein a processor within the plurality of processors includes a cache** 122, **a shared memory** 108, and **a bus** (connection shown in figure 1 between the network and between controller 106 of the node to the shared memory 108) **coupled between the plurality of processors and the shared memory, wherein the bus transports addresses and data between the shared memory and the plurality of processor** (necessarily inherent in the system of Ang as it is well known in the art that in order to access a location in a memory, an address is required and in order to receive requested data, the data must be retrieved from the memory and sent back to the requesting processor/hardware unit).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ang (U.S. Patent Application Publication No. 2003/0079085), as applied to claims 1-3,5,6,8-12,14,15, and 17-20, above.

As per claims 7 and 16, Ang does not specifically teach **wherein if a shared memory multiprocessor includes modules that are not able to switch to the write-broadcast protocol, locking the cache into the write-invalidate protocol**; however, such a limitation would have been obvious to one having ordinary skill in the art at the time the invention was made, as a given processor operating in the write-invalidate mode amongst other processors of a shared memory multiprocessor system operating in a write-update mode would pose a data integrity issue. Such obviousness is best set forth via an example. If cache line address A is currently shared among a first processor operating in a write-broadcast mode a second processor in a write-invalidate mode and the first processor modified address A, the first processor would also send out the updated data associated with address A (as discussed in the write-update protocol definition in Ang ¶3 and Applicant's ¶9). The second processor, not operating in the write-update mode would never receive the updated data (as it only awaits for invalidation messages to notify of shared cache line modifications) and instead assumes the data associated

with address A contained within its local cache is still valid. Therefore, when the second processor attempts to read from its local cache line address A, the data, as appears to the shared memory, is invalid as the first processor had already updated this data. Thus the data read by processor from its local cache would have been invalid.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the cache coherency protocol of Ang by locking the multiprocessor caches into a write-invalidate mode, if the cache (or portion thereof) of a particular processor of the multiprocessor shared memory system was not capable of switching to a write-broadcast protocol, thereby maintaining data integrity by way of keeping the caching policies among the plurality of processors in the multiprocessor shared memory system coherent with each other.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hosoya et al. (U.S. Patent No. 6,484,242) teaches determining whether or not a particular cache line is considered part of a "dedicated region" or a "common region" for applying a write-invalidation protocol or a write-update protocol (abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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